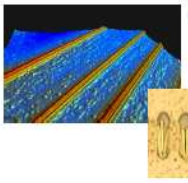
Future Challenges

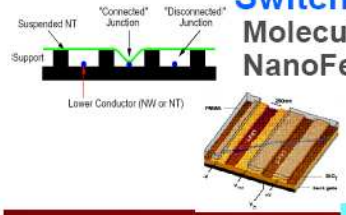
Bring On the Molecules!



Wires:
NanoTubes

+

Switches:
Molecular,
NanoFet



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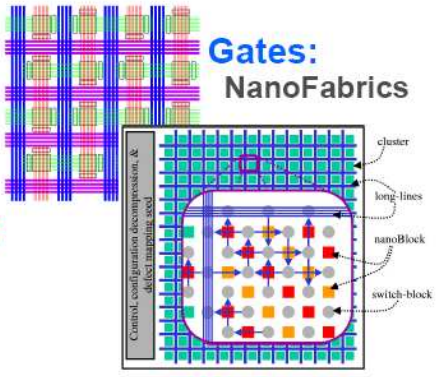

Gates:
NanoFabrics

GigaGate Capacity!

After: Butts, DeHon, and Goldstein (ICCAD 2002)

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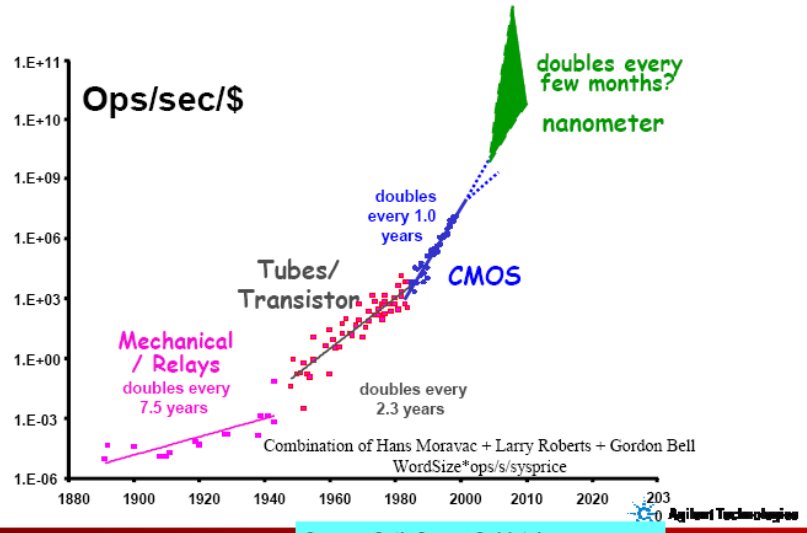
Moore's Law: You haven't seen anything yet!



Source: Seth Copen Goldstein (CMU)

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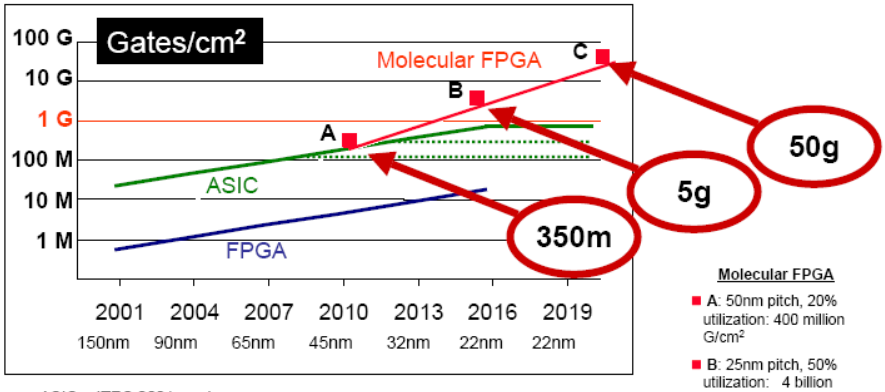
Logic Density Projections: the GigaGate Chip



- ASIC = ITRS 2001 roadmap
- FPGA = 8 transistor-area/crosspoint, 20 crosspoints/gate
- Molecular FPGA = 20 crosspoints/gate, assuming = ASIC in 2011, Moore's Law

Molecular FPGA

- A: 50nm pitch, 20% utilization: 400 million G/cm²
- B: 25nm pitch, 50% utilization: 4 billion G/cm²
- C: 10nm pitch, 80% utilization: 40 billion G/cm²

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Source: Michael Butts (Cadence)

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GigaGate Chip Design Challenges (2012)

- Assumptions:
  - Density: 300 MGate/cm^2 (1B Gate FPGA)
  - Productivity: 500 RTL gates/day (21%/yr ITRS)
- Implications
  - Design Effort: **1000 engineer-years**
  - Design Cost: **$150m** (@1m units = $150 / chip)

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